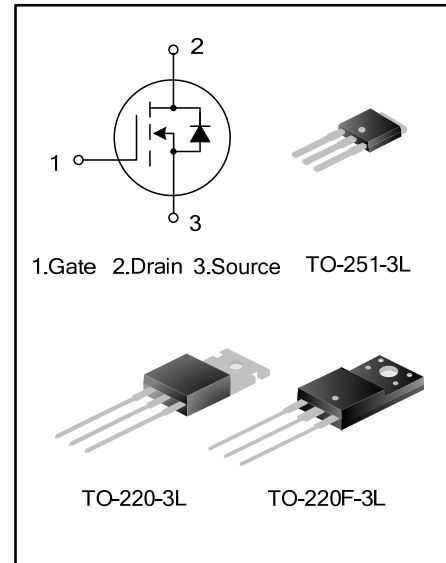


## 4A, 650V N-CHANNEL MOSFET

### GENERAL DESCRIPTION

SVF4N65T/F(G)/M is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

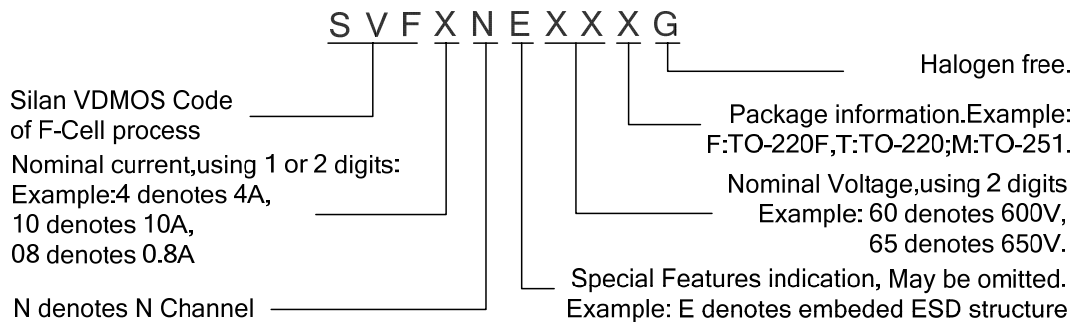
These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.



### FEATURES

- \* 4A,650V,  $R_{DS(on)(typ)}=2.5\Omega@V_{GS}=10V$
- \* Low gate charge
- \* Low Crss
- \* Fast switching
- \* Improved dv/dt capability

### NOMENCLATURE



### ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SVF4N65T	TO-220-3L	SVF4N65T	Pb free	Tube
SVF4N65F	TO-220F-3L	SVF4N65F	Pb free	Tube
SVF4N65FG	TO-220F-3L	SVF4N65FG	Halogen free	Tube
SVF4N65M	TO-251-3L	SVF4N65M	Pb free	Tube

**ABSOLUTE MAXIMUM RATINGS** ( $T_C=25^\circ\text{C}$  unless otherwise noted)

Characteristics	Symbol	Ratings			Unit
		SVF4N65T	SVF4N65F(G)	SVF4N65M	
Drain-Source Voltage	$V_{DS}$	650			V
Gate-Source Voltage	$V_{GS}$	$\pm 30$			V
Drain Current	$I_D$	$T_C=25^\circ\text{C}$			A
		$T_C=100^\circ\text{C}$			
Drain Current Pulsed	$I_{DM}$	16			A
Power Dissipation( $T_C=25^\circ\text{C}$ ) -Derate above $25^\circ\text{C}$	$P_D$	100	33	77	W
		0.80	0.26	0.62	W/ $^\circ\text{C}$
Single Pulsed Avalanche Energy (Note 1)	$E_{AS}$	202			mJ
Operation Junction Temperature Range	$T_J$	$-55 \sim +150$			$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	$-55 \sim +150$			$^\circ\text{C}$

**THERMAL CHARACTERISTICS**

Characteristics	Symbol	Ratings			Unit
		SVF4N65T	SVF4N65F(G)	SVF4N65M	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.25	3.79	1.62	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	120	110	$^\circ\text{C/W}$

**ELECTRICAL CHARACTERISTICS** ( $T_C=25^\circ\text{C}$  unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	$B_{V_{DSS}}$	$V_{GS}=0V, I_D=250\mu\text{A}$	650	--	--	V
Drain-Source Leakage Current	$I_{DSS}$	$V_{DS}=650V, V_{GS}=0V$	--	--	10	$\mu\text{A}$
Gate-Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 30V, V_{DS}=0V$	--	--	$\pm 100$	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu\text{A}$	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=2A$	--	2.5	2.7	$\Omega$
Input Capacitance	$C_{iss}$	$V_{DS}=25V, V_{GS}=0V,$ $f=1.0\text{MHZ}$	--	464	--	pF
Output Capacitance	$C_{oss}$		--	54	--	
Reverse Transfer Capacitance	$C_{rss}$		--	1.32	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=325V, I_D=4.0A,$ $R_G=25\Omega$  (Note 2,3)	--	16.6	--	ns
Turn-on Rise Time	$t_r$		--	37.33	--	
Turn-off Delay Time	$t_{d(off)}$		--	18.0	--	
Turn-off Fall Time	$t_f$		--	19.2	--	
Total Gate Charge	$Q_g$	$V_{DS}=520V, I_D=4.0A,$ $V_{GS}=10V$  (Note 2,3)	--	8.03	--	nC
Gate-Source Charge	$Q_{gs}$		--	2.57	--	
Gate-Drain Charge	$Q_{gd}$		--	3.03	--	

## SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	$I_S$	Integral Reverse P-N Junction Diode in the MOSFET	--	--	4.0	A
Pulsed Source Current	$I_{SM}$		--	--	16	
Diode Forward Voltage	$V_{SD}$	$I_S=4.0A, V_{GS}=0V$	--	--	1.4	V
Reverse Recovery Time	$T_{rr}$	$I_S=4.0A, V_{GS}=0V,$ $di_F/dt=100A/\mu s$	--	190	--	ns
Reverse Recovery Charge	$Q_{rr}$		--	0.53	--	$\mu C$

### Notes:

1.  $L=30mH, I_{AS}=3.36A, V_{DD}=150V, R_G=25\Omega,$  starting  $T_J=25^\circ C$ ;
2. Pulse Test: Pulse width  $\leq 300\mu s,$  Duty cycle  $\leq 2\%$ ;
3. Essentially independent of operating temperature.

**TYPICAL CHARACTERISTICS**

Figure 1. On-Region Characteristics

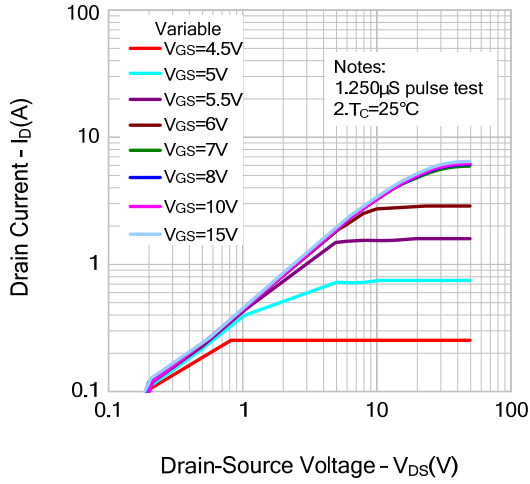


Figure 2. Transfer Characteristics

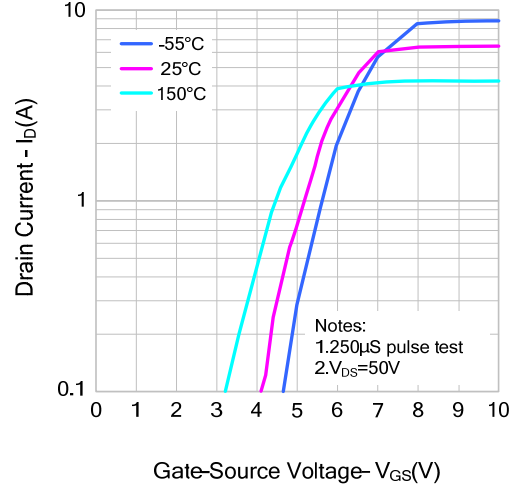


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

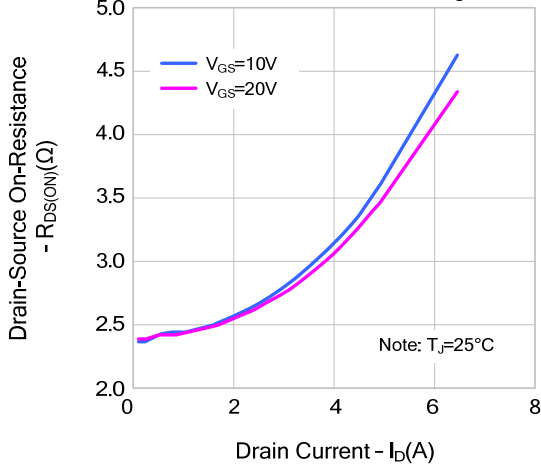


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

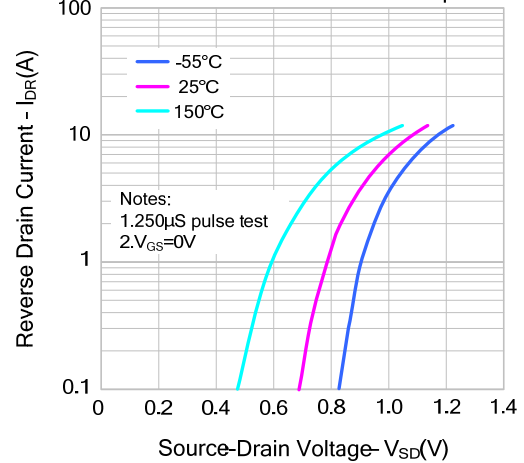


Figure 5. Capacitance Characteristics

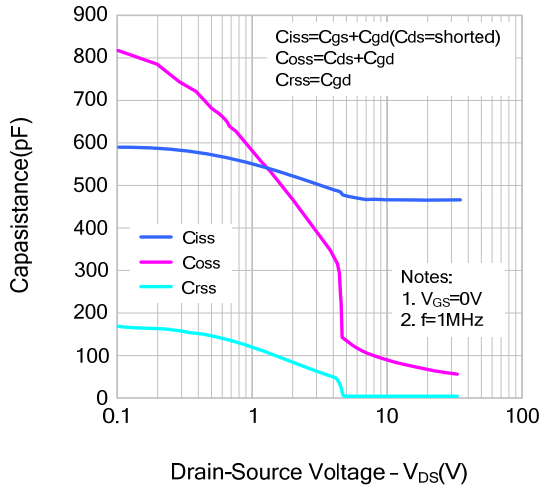
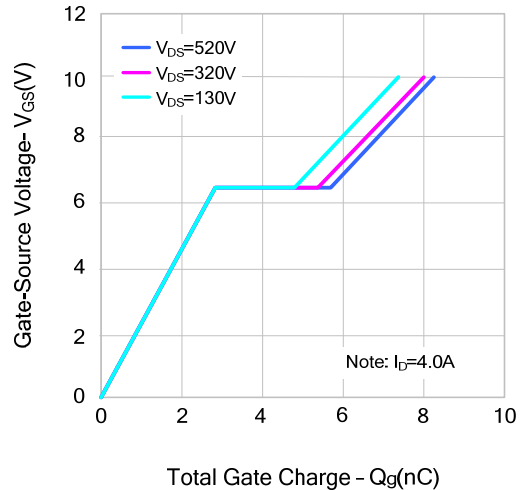


Figure 6. Gate Charge Characteristics



**TYPICAL CHARACTERISTICS(continued)**

Figure 7. Breakdown Voltage Variation vs. Temperature

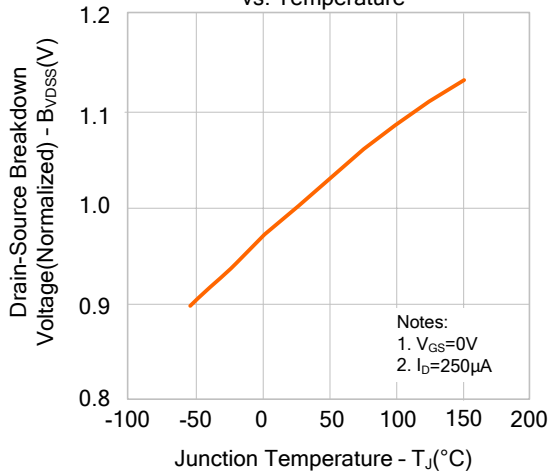


Figure 8. On-resistance Variation vs. Temperature

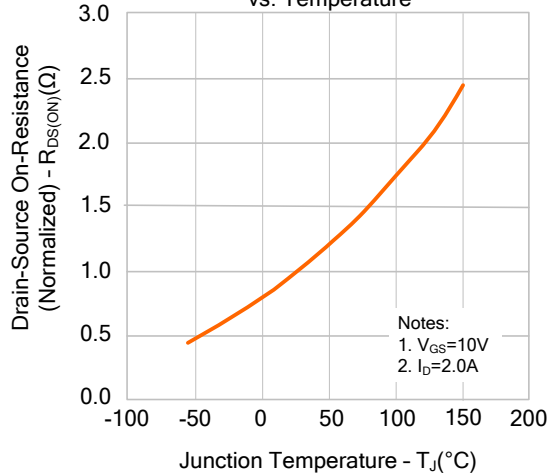


Figure 9-1. Max. Safe Operating Area(SVF4N65T)

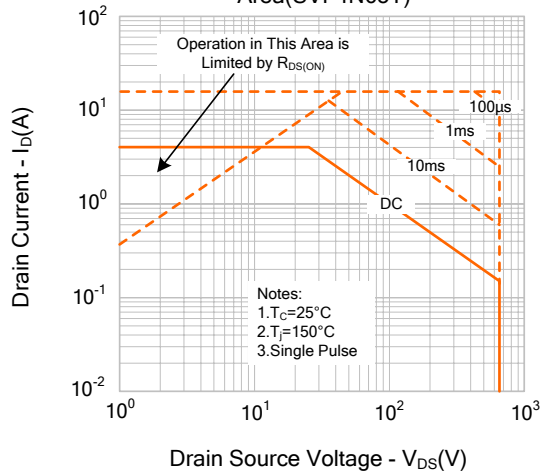


Figure 9-2. Max. Safe Operating Area(SVF4N65F(G))

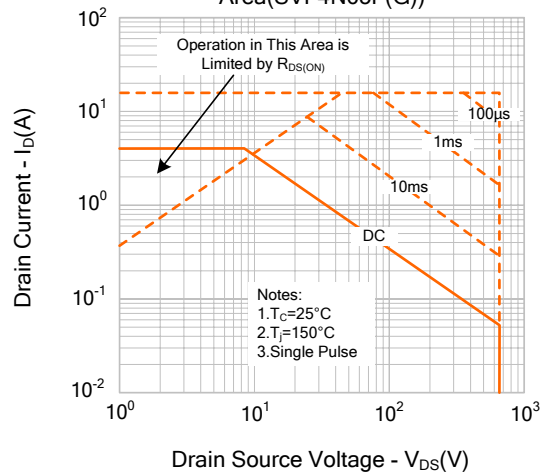


Figure 9-3. Max. Safe Operating Area(SVF4N65M)

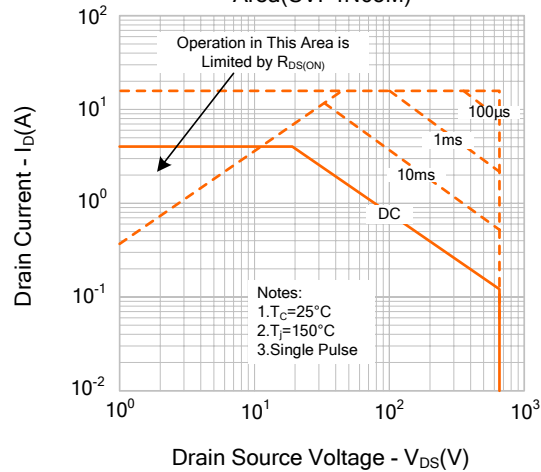
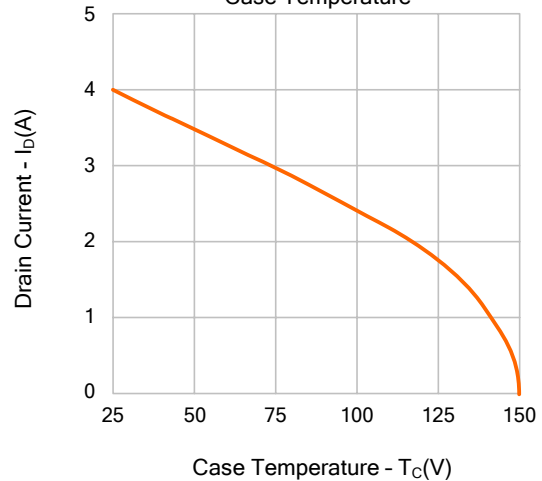
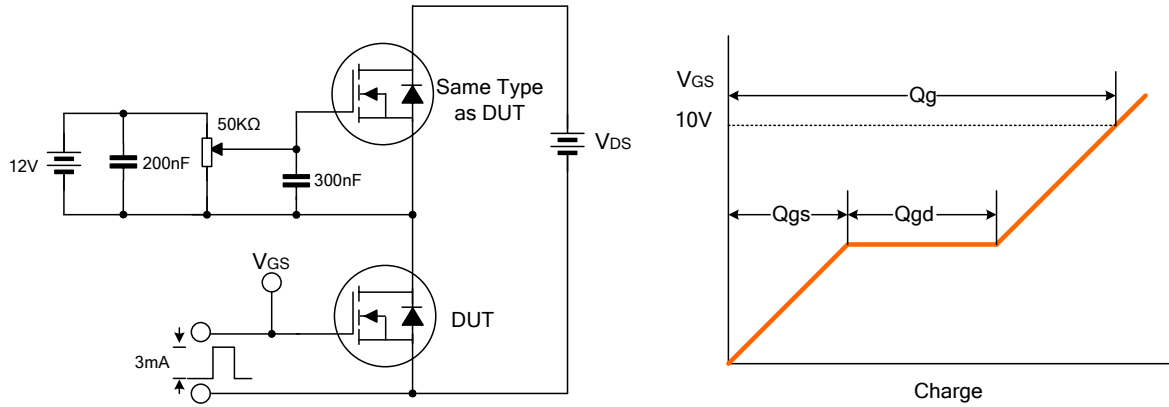


Figure 10. Maximum Drain Current vs. Case Temperature

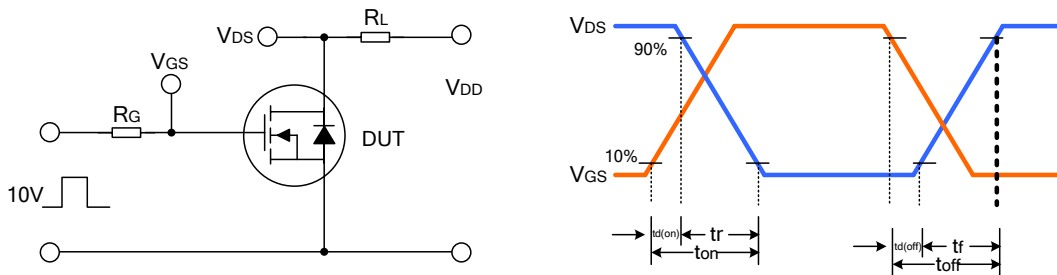


**TYPICAL TEST CIRCUIT**

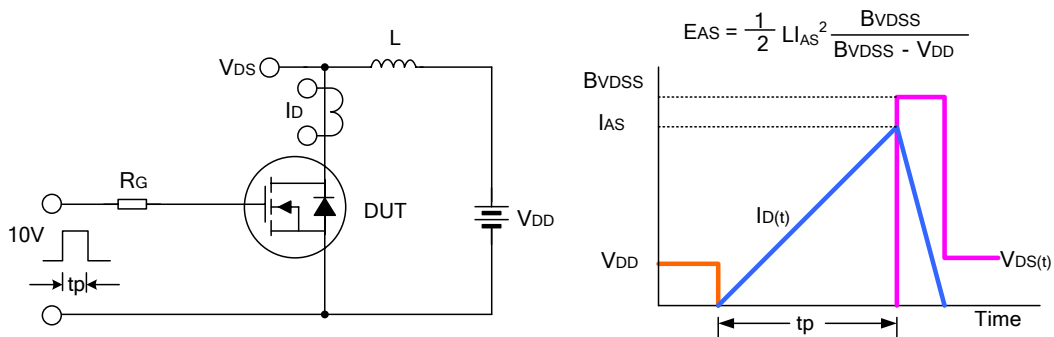
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



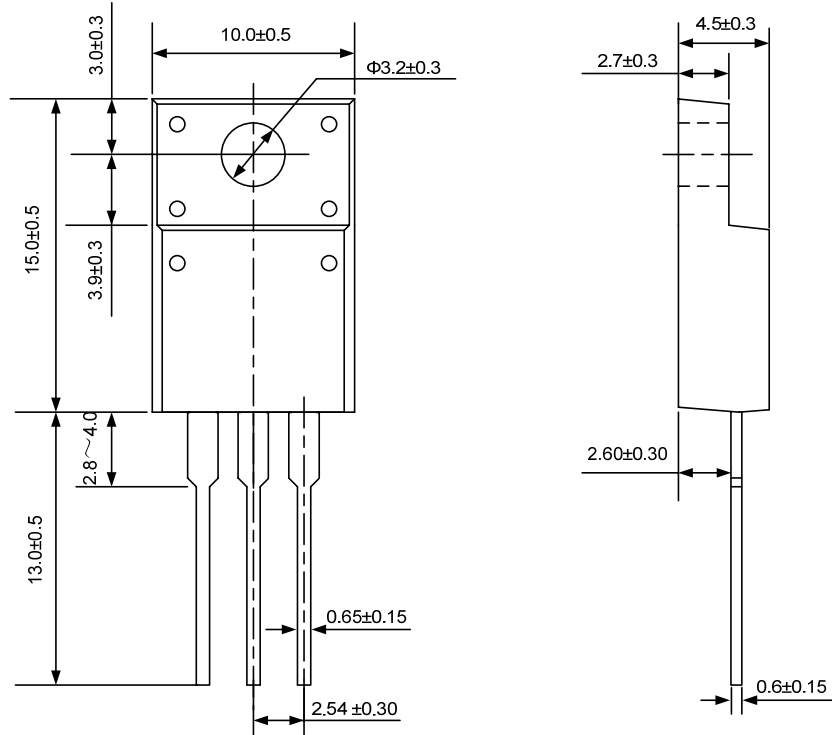
Unclamped Inductive Switching Test Circuit & Waveform



**PACKAGE OUTLINE**

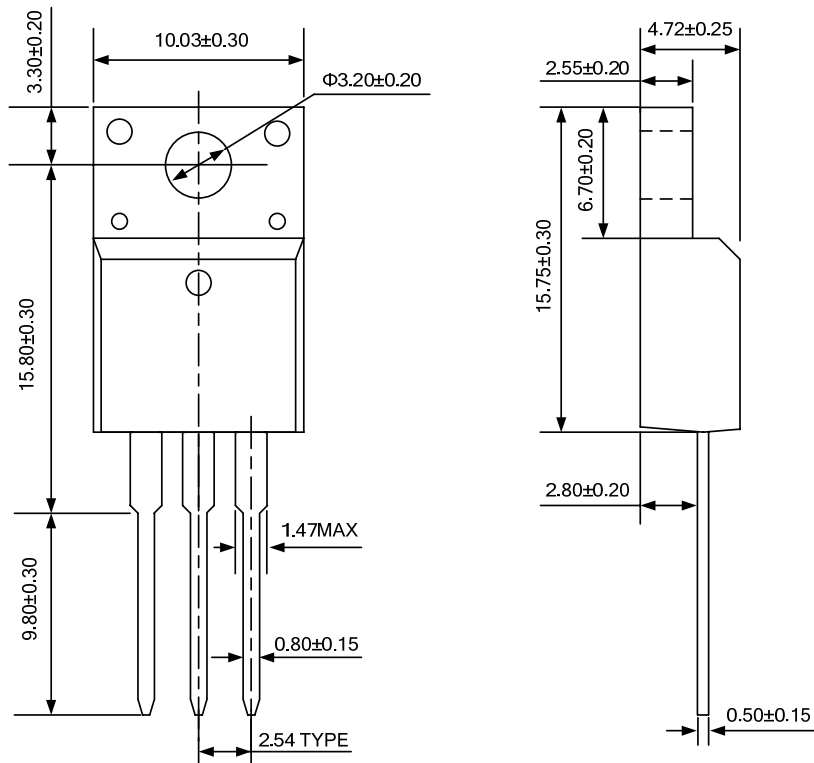
**TO-220F-3L(1)**

**UNIT: mm**



**TO-220F-3L(2)**

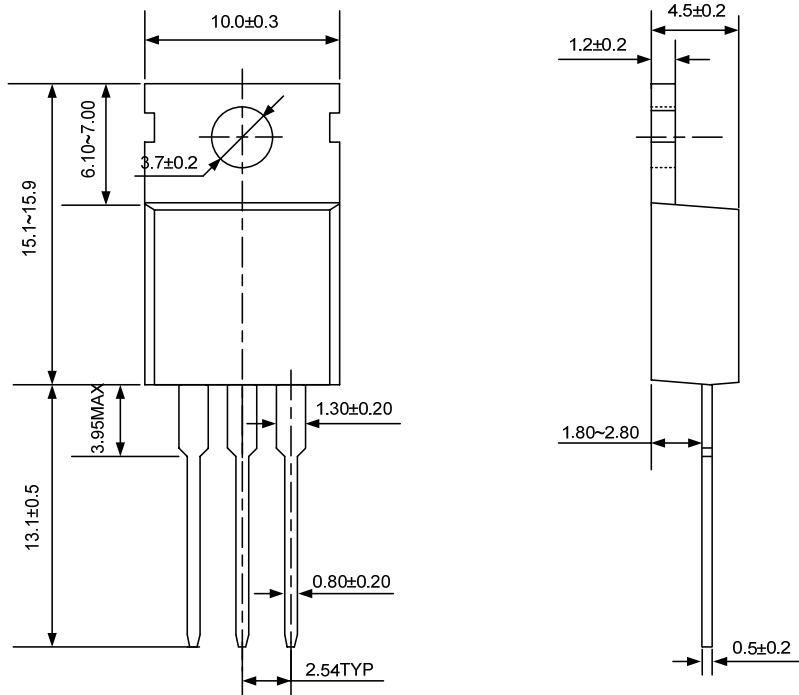
**UNIT: mm**



**PACKAGE OUTLINE (continued)**

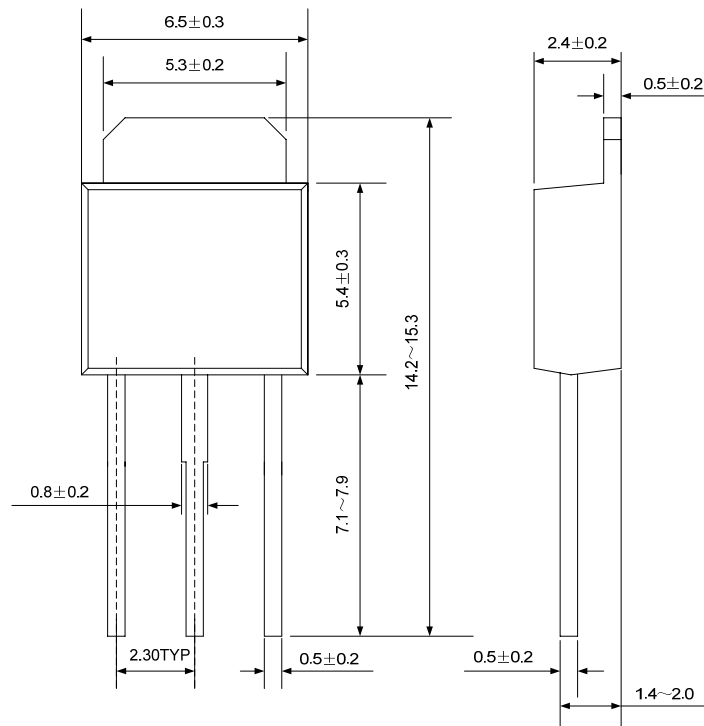
**TO-220-3L**

**UNIT: mm**



**TO-251-3L**

**UNIT: mm**







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- Silan will supply the best possible product for customers!

## ATTACHMENT

### Revision History

Date	REV	Description	Page
2011.01.18	1.0	Original	