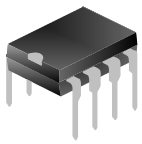
CURRENT MODE PWM+PFM CONTROLLER WITH BUILT-IN HIGH VOLTAGE MOSFET

DESCRIPTION

SD686X is current mode PWM+PFM controller with built-in high-voltage MOSFET used for SMPS, with low standby power and low start current for power switch. In standby mode, the circuit enters burst mode to reduce the standby power dissipation. The switch frequency is 25~67KHz with jitter frequency for low EMI.

Built-in peak current compensation circuit makes the limit peak current stable even with different input AC voltage. Limit output power can be adjusted through the resistor. Maximum peak current compensation during power-on reduces pressure on transformer to avoid saturation, the peak current compensation will decrease for balance after power-on.

It integrates various protections such as undervoltage lockout, overvoltage protection, overload protection, lead edge blanking, primary winding overcurrent protection and thermal shutdown. The circuit will restart until normal if protection occurs.



DIP-8-300-2.54

APPLICATIONS

* SMPS

FEATURES

* Energy Star 2.0 standard
* Lower start-up current (3μA)
* Various switching frequency following load for the higher efficiency
* Frequency jitter for low EMI
* Overvoltage, primary winding overcurrent, overload and over temperature protections.
* Adjustable limit output power
* Undervoltage lockout
* Built-in high voltage MOSFET
* Auto restart mode
* Peak current compensation
* Maximum peak current compensation for initialization to realize the soft start function.
* Burst mode
* Cycle by cycle current limit

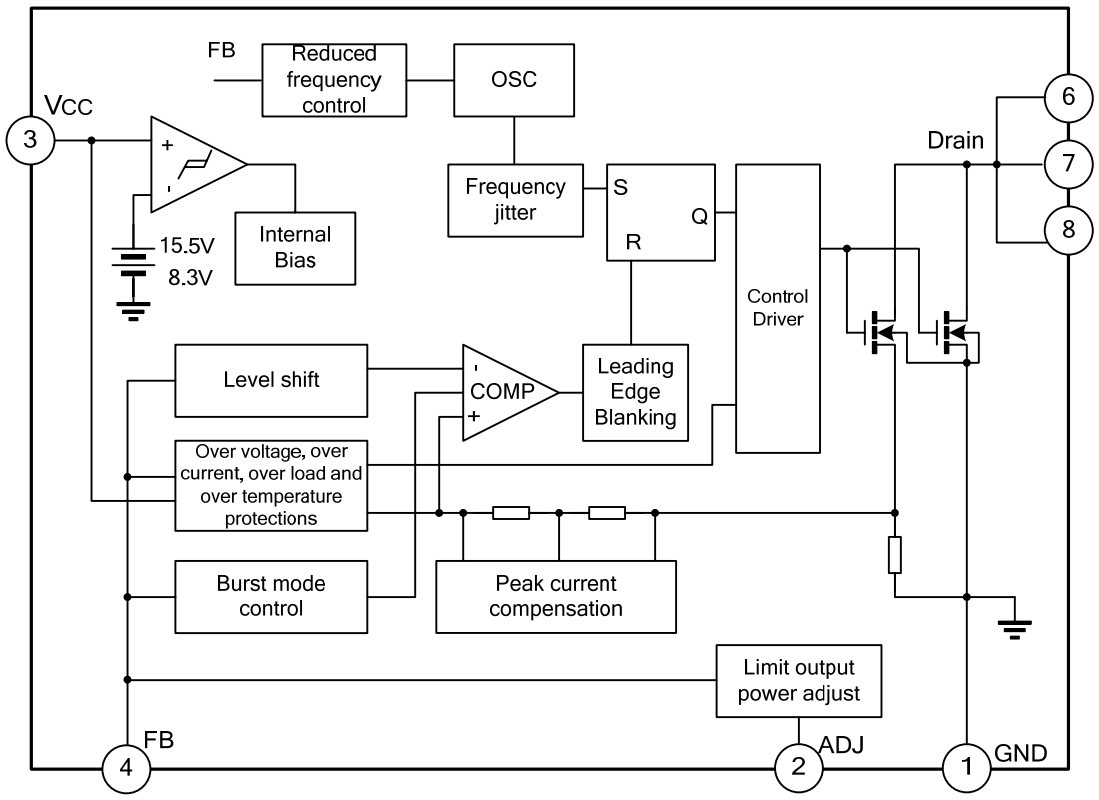
ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SD6860	DIP-8-300-2.54	SD6860	Pb free	Tube
SD6861/SD6861G		SD6861/SD6861G	Pb free/Halogen free	Tube
SD6862		SD6862	Pb free	Tube
SD6863/SD6863G		SD6863/SD6863G	Pb free/Halogen free	Tube
SD6864/SD6864G		SD6864/SD6864G	Pb free/Halogen free	Tube

TYPICAL OUPUT POWER CAPABILITY

Part No.	190~265V		85~265V	
	Adapter	Open	Adapter	Open
SD6860	7W	9W	5W	7.2W
SD6861/SD6861G	10W	14W	8W	12W
SD6862	12W	17W	10W	14W
SD6863/SD6863G	14W	19W	12W	15W
SD6864/SD6864G	16W	21W	14W	18W

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING(unless otherwise specified, T_{amb}=25°C)

Characteristics		Symbol	Rating	Unit
Drain-Gate Voltage (R_{GS}=1MΩ)		V_{DGR}	650	V
Gate-Source (GND) Voltage		V_{GS}	±30	V
Drain Current Pulse note1	SD6860	I_{DM}	4	A
	SD6861/SD6861G		6	
	SD6862		8	
	SD6863/SD6863G		10	
	SD6864/SD6864G		14	
Continuous Drain Current (Tamb=25°C)	SD6860	I_D	0.8	A
	SD6861/SD6861G		1	
	SD6862		2	
	SD6863/SD6863G		2.5	
	SD6864/SD6864G		3.5	
Signal Pulse Avalanche Energy note2	SD6860	E_{AS}	15	mJ
	SD6861/SD6861G		30	
	SD6862		68	
	SD6863/SD6863G		140	
	SD6864/SD6864G		200	
Power Supply Voltage		$V_{CC,MAX}$	28	V
Feedback input voltage		V_{FB}	-0.3~7	V
Limit output power voltage		V_{ADJ}	-0.3~2	V
Allowable Power Dissipation		P_D	6.3	W
Ambient thermal resistance		θ_{ja}	77	°C/W
Surface thermal resistance		θ_{jc}	20	°C/W
Operating Junction Temperature		T_J	+150	°C
Operating Temperature Range		T_{amb}	-25~+85	°C
Storage Temperature Range		T_{STG}	-55~+150	°C

Note: 1. Pulse width is limited by maximum junction temperature;

2. L=51mH, T_J=25°C(start).

ELECTRICAL CHARACTERISTICS (for MOSFET, unless otherwise specified, T_{amb}=25°C)

Characteristics		Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS}=0V, I_D=50μA	650	--	--	V
Zero Gate Voltage Drain Current		I_{DSS}	V_{DS}=650V, V_{GS}=0V	--	--	50	μA
			V_{DS}=480V,V_{GS}=0V,T_{amb}=125°C	--	--	200	μA
Static Drain-Source On Resistance	SD6860	$R_{DS(ON)}$	V_{GS}=10V, I_D=0.5A	9.1	13	16.9	Ω
			V_{GS} =10V, I_D =0.75A	9.4	13.5	17.6	
	SD6861/SD6861G		V_{GS} =10V, I_D =0.5A	7	10	13	
			V_{GS} =10V, I_D =0.75A	7.3	10.5	13.7	
	SD6862		V_{GS} =10V, I_D =0.5A	3.9	5.6	7.3	
			V_{GS} =10V, I_D =1.0A	4.0	5.8	7.6	
	SD6863/SD6863G		V_{GS} =10V I_D =0.5A	2.3	3.4	4.5	
			V_{GS} =10V, I_D =1.25A	2.5	3.6	4.7	
	SD6864/SD6864G		V_{GS} =10V, I_D =0.5A	1.7	2.5	3.3	
			V_{GS} =10V, I_D =1.5A	1.8	2.6	3.4	
			V_{GS} =10V, I_D =1.75A	1.8	2.7	3.6	
Input Capacitance	SD6860	C_{ISS}	V_{GS}=0V, V_{DS}=25V, f=1MHz	84	121	157	pF
	SD6861/SD6861G			108	155	202	
	SD6862			182	260	338	
	SD6863/SD6863G			224	320	416	
	SD6864/SD6864G			305	435	566	
Output Capacitance	SD6860	C_{OSS}	V_{GS}=0V, V_{DS}=25V, f=1MHz	13	19	25	pF
	SD6861/SD6861G			16	23	30	
	SD6862			27	39	51	
	SD6863/SD6863G			28	41	54	
	SD6864/SD6864G			37	53	69	
Reverse Transfer Capacitance	SD6860	C_{RSS}	V_{GS}=0V, V_{DS}=25V, f=1MHz	0.4	0.6	0.8	pF
	SD6861/SD6861G			0.4	0.6	0.8	
	SD6862			0.7	1.0	1.3	
	SD6863/SD6863G			0.9	1.3	1.7	
	SD6864/SD6864G			0.9	1.4	1.9	
Turn On Delay Time	SD6860	$T_{D(ON)}$	V_{DD}=0.5BV_{DSS}, I_D=25mA	4.2	6	7.8	ns
	SD6861/SD6861G			4.2	6	7.8	
	SD6862			7.7	11	14.3	
	SD6863/SD6863G			9.1	13	16.9	
	SD6864/SD6864G			11.2	16	20.8	
Rise Time	SD6860	T_R	V_{DD}=0.5BV_{DSS}, I_D=25mA	7.7	11	14.3	ns
	SD6861/SD6861G			9.1	13	16.9	
	SD6862			18.2	26	33.8	
	SD6863/SD6863G			21.7	31	40.3	
	SD6864/SD6864G			25.2	36	46.8	

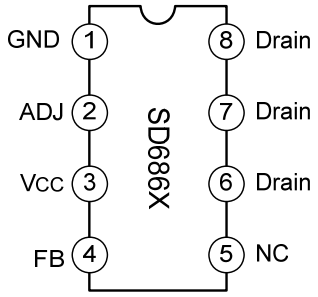
Characteristics		Symbol	Test conditions	Min.	Typ.	Max.	Unit
Turn Off Delay Time	SD6860	$T_{D(OFF)}$	V_{DD}=0.5BV_{DSS}, I_D=25mA	5.6	8	10.4	ns
	SD6861/SD6861G			6.3	9	11.7	
	SD6862			11.9	17	22.1	
	SD6863/SD6863G			12.6	18	23.4	
	SD6864/SD6864G			11.9	17	22.1	
Fall Time	SD6860	T_F	V_{DD}=0.5BV_{DSS}, I_D=25mA	10.5	15	19.5	ns
	SD6861/SD6861G			11.9	17	22.1	
	SD6862			13.3	19	24.7	
	SD6863/SD6863G			14	20	26	
	SD6864/SD6864G			12.6	18	23.4	

ELECTRICAL CHARACTERISTICS (unless otherwise specified, V_{CC}=12V, T_{amb}=25°C)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Undervoltage Section						
Start Threshold Voltage	V_{START}		14.5	15.5	17	V
Stop Threshold Voltage	V_{STOP}		7.5	8.3	9.5	V
Oscillator Section						
Max. Oscillate Frequency	f_{OSCMAX}	VFB=3V	61	67	73	KHz
Min. Oscillate Frequency	f_{OSCMIN}	V_{BURL}<V_{FB}<V_{BURH}	20	25	30	KHz
Frequency jitter	f_{MOD}	Oscillate frequency is the maximum	±1.5	±2.5	±3.5	KHz
Frequency Change With Temperature	--	25°C≤T_{amb}≤+85°C	--	±5	±10	%
Maximum Duty cycle	D_{MAX}		72	77	82	%
Feedback Section						
MAX. Feedback Source Current	I_{FBMAX}	V_{FB}=0V, R_{ADJ}=0	0.8	0.9	1.0	mA
Shutdown Feedback Voltage (over load protection)	V_{SD}		3.8	4.3	4.8	V
Shutdown Feedback Delay Time	T_{SD}	FB is increased to 5V from 0V instantly	15	27	40	ms
Shutdown Delay Current	I_{DELAY}	V_{FB}=5V	3	5.5	8	μA
Limit Output power						
FB current 1	I_{FB1}	V_{FB}=0V, R_{ADJ}=200KΩ	0.57	0.65	0.73	mA
Min. Resistor For Limit Output Power Adjust	R_{ADJ}	V_{FB}=0V, FB current is decreased	70	90	110	KΩ
Current Limit						
Peak Current Limit	SD6860	I_{OVER}	0.53	0.60	0.67	A
	SD6861/SD6861G		0.67	0.75	0.83	
	SD6862		0.80	0.90	1.00	
	SD6863/SD6863G		1.10	1.20	1.30	
	SD6864/SD6864G		1.35	1.50	1.65	

Characteristics		Symbol	Test conditions	Min.	Typ.	Max.	Unit
Burst mode							
Burst Mode High Voltage		V_{BURH}	FB voltage	0.40	0.50	0.60	V
Burst Mode Low Voltage		V_{BURL}	FB voltage	0.25	0.35	0.45	V
Protection Section							
Overvoltage Protection		V_{OVP}	V_{CC} voltage	23	24.5	26	V
Over temperature protection		T_{OTP}		125	150	175	°C
Leading-edge Blanking Time		T_{LEB}		250	325	450	ns
Total Standby Current							
Start Current		I_{START}	V_{CC} increases from 0V to 12V	1	3	10	μA
Quiescent Current		I_{STATIC}	V_{FB}=0V	1.0	1.9	3.0	mA
Operating Current	SD6860	I_{OP}	V_{FB}=3V	1.0	2.0	3.0	mA
	SD6861/SD6861G			1.0	2.0	3.0	mA
	SD6862			1.2	2.2	3.2	mA
	SD6863/SD6863G			1.2	2.2	3.2	mA
	SD6864/SD6864G			1.4	2.4	3.4	mA

PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Function description
1	GND	I	Ground
2	ADJ	I	ADJ pin
3	Vcc	I	Power supply pin
4	FB	I/O	Feedback input pin
5	NC	-	NC
6, 7, 8	Drain	O	Drain pins.

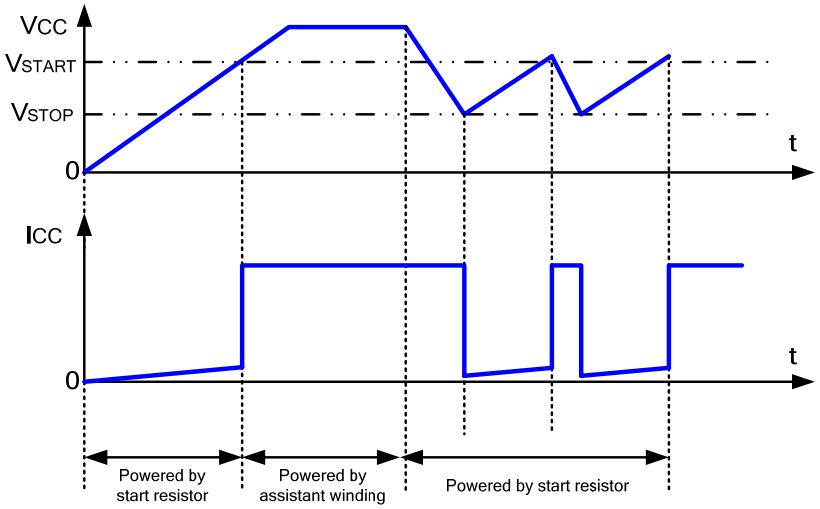
FUNCTION DESCRIPTION

SD686X is designed for off-line SMPS, consisting of high voltage MOSFET, optimized gate driver and current mode PWM+PFM controller which includes frequency oscillator and various protections such as undervoltage lockout, overvoltage protection and overload protection. Frequency jitter generated from oscillator is used to lower EMI. Burst mode is adopted during light load to lower standby power dissipation,

and function of lead edge blanking eliminates the MOSFET error shutdown caused by interference through minimizing MOSFET turning on time. Peak current compensation reduces the pressure on transformer during circuit starts and output power limit can be adjusted by resistor through ADJ pin. Few peripheral components are needed for higher efficiency and higher reliability and it is suitable for flyback converter and forward converter.

1. Under Voltage Lockout and Self-Start

At the beginning, the capacitor connected to pin V_{CC} is charged via start resistor by high voltage AC and the circuit starts to work if voltage at V_{CC} is 15.5V. The output and FB source current are shutdown if there is any protection during normal operation and V_{CC} is decreased because of powering of auxiliary winding. The whole control circuit is shutdown if voltage at V_{CC} is 8.3V below to lower current dissipation and the capacitor is recharged for restarting.

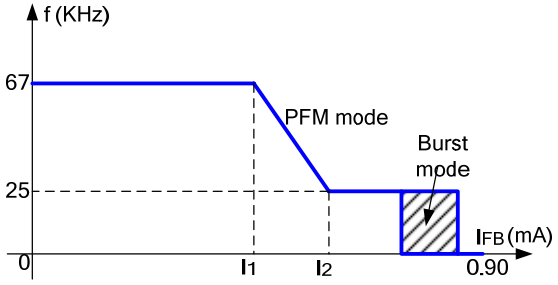


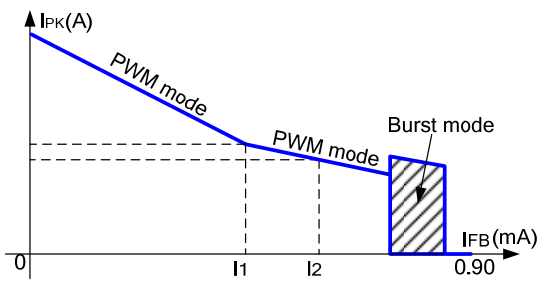
2. Frequency Jitter and reduced frequency mode

The oscillation frequency is kept changed for low EMI and decreasing radiation on one frequency. The oscillation frequency changes within a very small range to simplify EMI design. The rule of frequency changing (frequency center is 67KHz): ±2.5KHz change in 4ms, 63 frequency points in all.

For high efficiency, reduced frequency mode is adopted with two methods:

1. Frequency is reduced according to current output from FB pin. If output power has not been adjusted, that is $R_{ADJ} \leq 90K\Omega$, when I_{FB} value raises to I_1, frequency starts to be reduced from 67KHz and reduced to 25KHz (typ.) when I_{FB} is I_2, the change is shown below.
2. I_{PK} is changed according to I_{FB}, shown below.





3. Peak current compensation and normalization

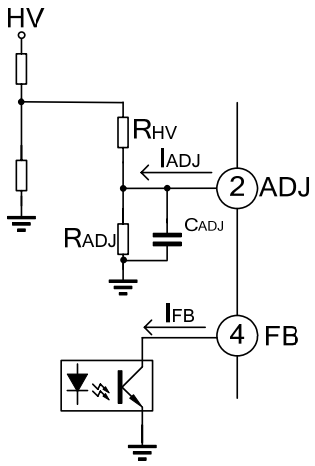
Generally, limit peak current changes with different inputs. Limit peak current is hold in this circuit because of peak current compensation. Larger peak current compensation for higher input AC voltage, it decreases to zero with light load and no peak current compensation in burse mode.

Maximum peak current compensation during power-on reduces pressure on transformer to avoid saturation, the peak current compensation will decrease for balance after power-on. The duration is decided by the load.

4. Limit output power adjust

Limit output power is adjusted by varying FB current through resistor R_{ADJ} adjust. When R_{ADJ}=0, no change in limit output power; when R_{ADJ} exceeds typ. 90KΩ, limit output power begins to be reduced.

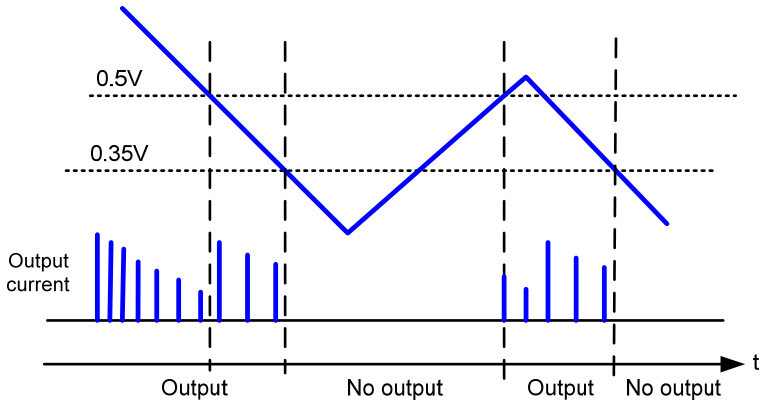
Moreover, limit output power can be kept stable (under different HV conditions) through pin ADJ, shown below.



5. Burst mode

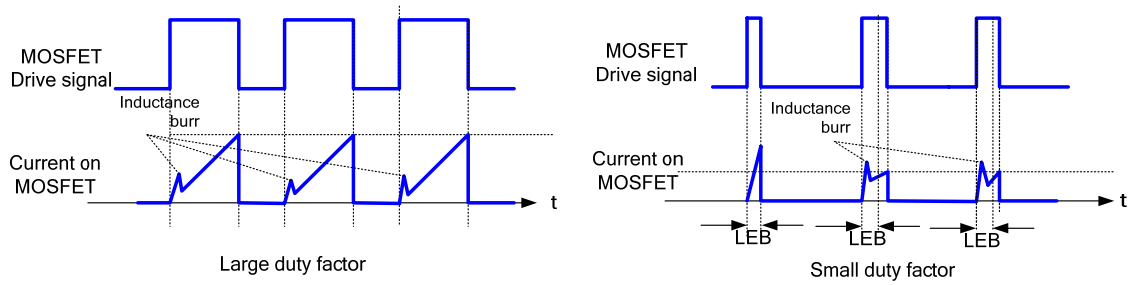
Working in this mode to reduce the power dissipation. It works normally when FB is 0.5V above, and during 0.35V<FB <0.5V, there are two different conditions: when FB changes from low to high, there is no action for switch and it is the same with condition of FB lower than 0.35V; the other is that FB changes form high to low, comparison value is increased for increasing turning on time to decrease switch loss. In this mode, switching frequency is down to 25KHz.

For this mode, during FB changes form high to low, the output voltage increases (increasing speed is decided by load) because of the high comparison value to decrease FB until it is 0.35V below; when FB <0.35V, there is no action for switch and output voltage decrease (decreasing speed is also decided by load) to increase FB voltage. FB voltage is 0.5V below with light load. This is repeated to decrease action of switch for lower power dissipation.



6. Leading Edge Blanking

For this current-controlled circuit, there is pulse peak current during the transient of switch turning on and there is an error operation if the current is sampled during this time. And leading edge blanking is adopted to eliminate this error operation. The output of PWM comparator is used for controlling shutdown after the leading edge blanking if there is any output drive.



7. Over Voltage Protection

The output is shutdown if voltage at V_{CC} exceeds the threshold value and this state is kept until the circuit is powered on reset.

8. Overload Protection

FB voltage increases if there is overload and the output is shutdown when FB voltage is up to the feedback shutdown voltage. This state is kept until the circuit is powered on reset.

9. Cycle By Cycle Peak Current Limit

During each cycle, the peak current value is decided by the comparison value of the comparator, which will not exceed the peak current limited value to guarantee the current on MOSFET will not be larger than the rating current. The output power will not increase if the current reaches the peak value to limit the max. output power.

The output voltage decreases and FB voltage increases if there is overload and corresponding protection occurs.

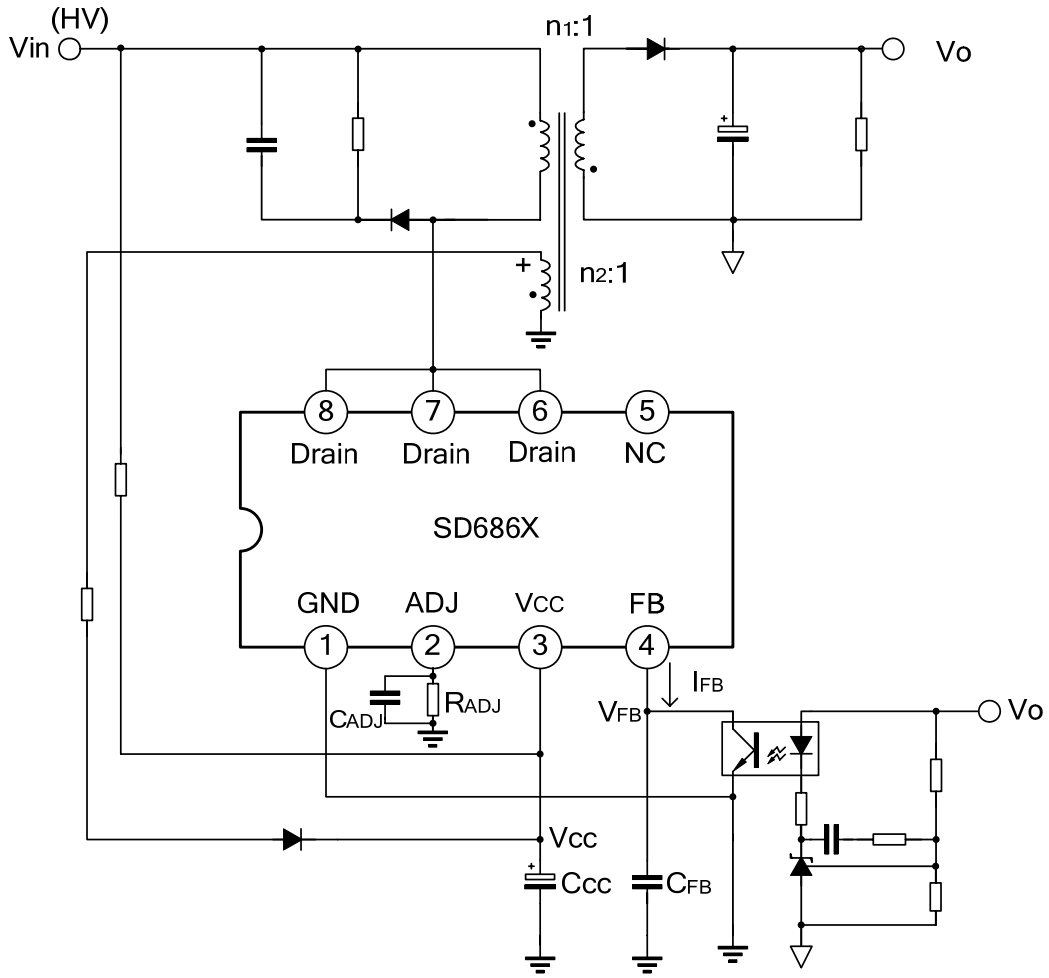
10. Primary winding over current protection

If secondary diode is short, or the transformer is short, this protection will occur. At this time, once it is over current in spite of the leading edge blanking (L.E.B) time, protection will begin after 300ns, and is active for every cycle. When the voltage on the current sense resistor is 1.7V, this protection will occur and the output is shut down. This state is kept until the under voltage occurs, and the circuit will start.

11. Thermal Shutdown

If the circuit is over temperature, the over temperature protection will shut down the output to prevent the circuit from damage. This state keeps until the circuit restarts after cooling down.

TYPICAL APPLICATION CIRCUIT

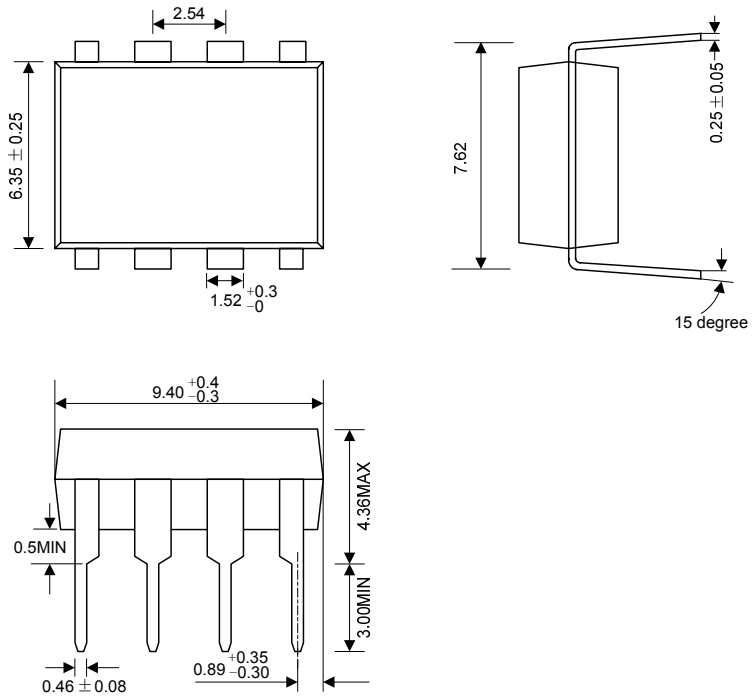


Note:

The circuit and parameters are for reference only, please set the parameters of the real application circuit based on the real test.

PACKAGE OUTLINE

DIP-8-300-2.54 UNIT: mm



MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

ATTACHMENT

Revision History

Date	REV	Description	Page
2010.03.12	1.0	Original	
2010.05.18	1.1	Modify ”DESCRIPTION”, ”FEATURES”, ”BLOCK DIAGRAM”, ”ABSOLUTE MAXIMUM RATING”, ”ELECTRICAL CHARACTERISTICS”, ”PIN CONFIGURATION”, ”PIN DESCRIPTION”, ”FUNCTION DESCRIPTION”, ”TYPICAL APPLICATION CIRCUIT”	
2010.05.26	1.2	Modify ”TYPICAL APPLICATION CIRCUIT”	10
2010.06.23	1.3	Modify ”TYPICAL OUPUT POWER CAPABILITY”; Delete the suffix of “Part No. “	2
2010.10.14	1.4	Modify SWPS to SMPS	
2010.10.22	1.5	Modify template of datasheet	
2011.05.30	1.6	Modify “ABSOLUTE MAXIMUM RATING” Modify “ELECTRICAL CHARACTERISTICS”	3 5
2011.07.20	1.7	Modify “ABSOLUTE MAXIMUM RATING” Modify “ELECTRICAL CHARACTERISTICS”	3 4~6
2011.10.19	1.8	Modify ”BLOCK DIAGRAM”, Modify ”ABSOLUTE MAXIMUM RATING”, Modify “ELECTRICAL CHARACTERISTICS” Modify “PACKAGE OUTLINE”	2 3 6 11
2011.12.13	1.9	Modify “Start Threshold Voltage”	5
2012.02.24	2.0	Modify “ORDERING INFORMATION” Modify “ELECTRICAL CHARACTERISTICS(for MOSFET)” Modify “ELECTRICAL CHARACTERISTICS”	