# 10A, 600V N-CHANNEL MOSFET

GENERAL DESCRIPTION

SVF10N60T/F is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell^{TM} structure DMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.
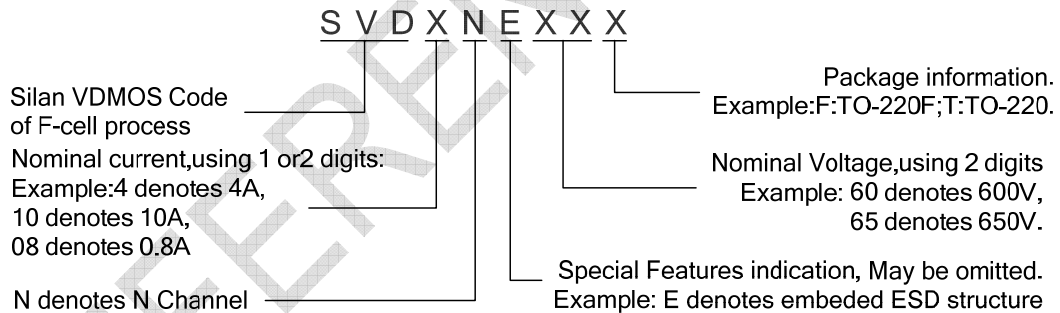
These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.
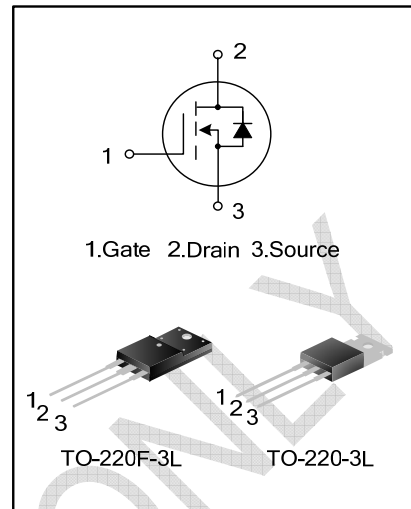
FEATURES

* 10A,600V,$R_{DS(on)(typ.)}$=0.78Ω@V_{GS}=10V
* Low gate charge
* Low Crss
* Fast switching
* Improved dv/dt capability

1.Gate 2.Drain 3.Source

TO-220F-3L   TO-220-3L

NOMENCLATURE

S V D X N E X X X

Silan VDMOS Code of F-cell process
Nominal current,using 1 or2 digits:
Example:4 denotes 4A,
10 denotes 10A,
08 denotes 0.8A

N denotes N Channel

Special Features indication, May be omitted.
Example: E denotes embedded ESD structure

Nominal Voltage,using 2 digits
Example: 60 denotes 600V,
65 denotes 650V.

Package information.
Example:F:TO-220F;T:TO-220.

ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SVF10N60T	TO-220-3L	SVF10N60T	Pb free	Tube
SVF10N60F	TO-220F-3L	SVF10N60F	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Parameter	Symbol	Rating		Unit
		SVF10N60T	SVF10N60F	
Drain-Source Voltage	V_{DS}	600		V
Gate-Source Voltage	V_{GS}	±30		V
Drain Current	I_D	10		A
Drain Current Pulsed	I_{DM}	40		A
Power Dissipation(T_C=25°C)	P_D	156	50	W
-Derate above 25°C		1.25	0.4	W/°C
Single Pulsed Avalanche Energy (Note 1)	E_{AS}	965		mJ
Operation Junction Temperature	T_J	150		°C
Storage Temperature	T_{stg}	-55～+150		°C

THERMAL CHARACTERISTICS

Parameter	Symbol	Rating		Unit
		SVF10N60T	SVF10N60F	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.8	2.5	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	120	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

| Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B_{VDSS}	V_{GS}=0V, I_D=250µA	600	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=600V, V_{GS}=0V	--	--	10	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250µA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=5.0A	--	0.78	1.0	Ω
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V, f=1.0MHZ	--	1498	--	pF
Output Capacitance	C_{oss}		--	156	--	
Reverse Transfer Capacitance	C_{rss}		--	16.8	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=300V,I_D=10A, R_G=25Ω	--	24.3	--	ns
Turn-on Rise Time	t_r		--	72	--	
Turn-off Delay Time	$t_{d(off)}$		--	137	--	
Turn-off Fall Time	t_f	(Note 2,3)	--	64	--	
Total Gate Charge	Q_g	V_{DS}=480V,I_D=10A, V_{GS}=10V	--	41.2	--	nC
Gate-Source Charge	Q_{gs}		--	7.6	--	
Gate-Drain Charge	Q_{gd}	(Note 2,3)	--	13.6	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse p-n Junction Diode in the MOSFET	--	--	10	A
Pulsed Source Current	I_{SM}		--	--	40	
Diode Forward Voltage	V_{SD}	I_S=10A,V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=10A,V_{GS}=0V,	--	407	--	ns
Reverse Recovery Charge	Q_{rr}	dI_F/dt=100A/µS (Note 2)	--	4.0	--	µC

Notes:

1. L=30mH, I_{AS}=6.6A, V_{DD}=215V, R_G=25Ω, starting T_J=25°C;

2. Pulse Test: Pulse width ≤300µs,Duty cycle≤2%;

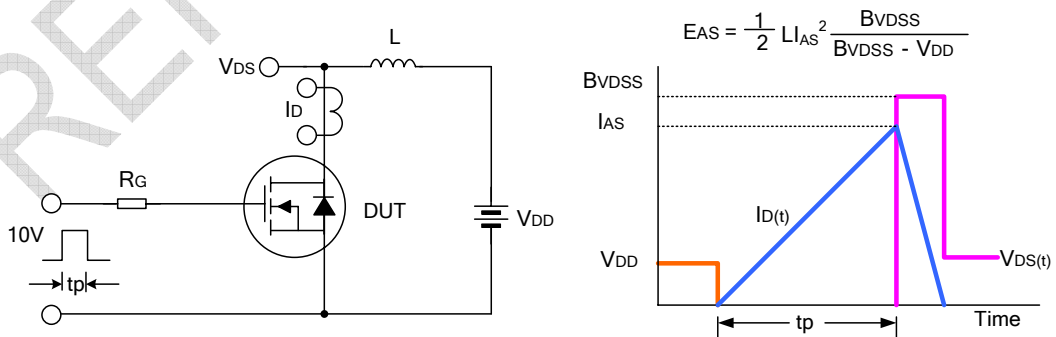3. Essentially independent of operating temperature.

TYPICAL TEST CIRCUIT

Gate Charge Test Circuit & Waveform
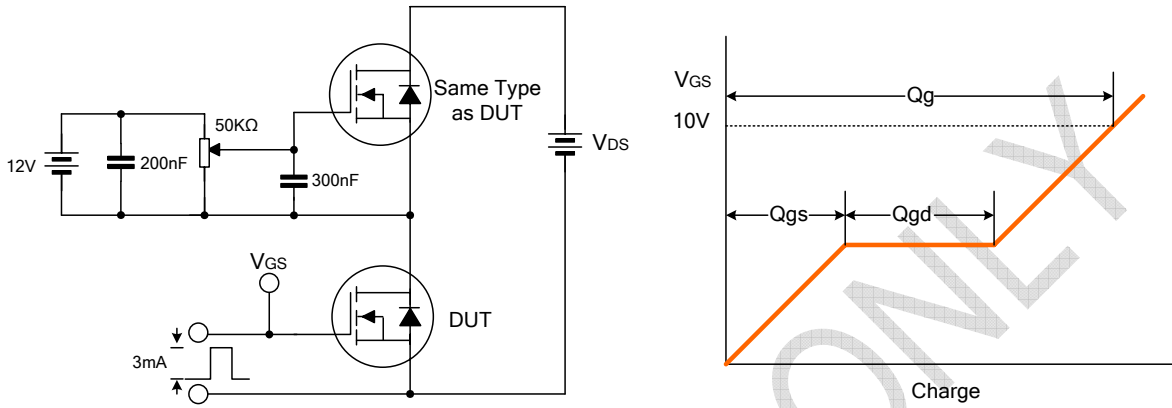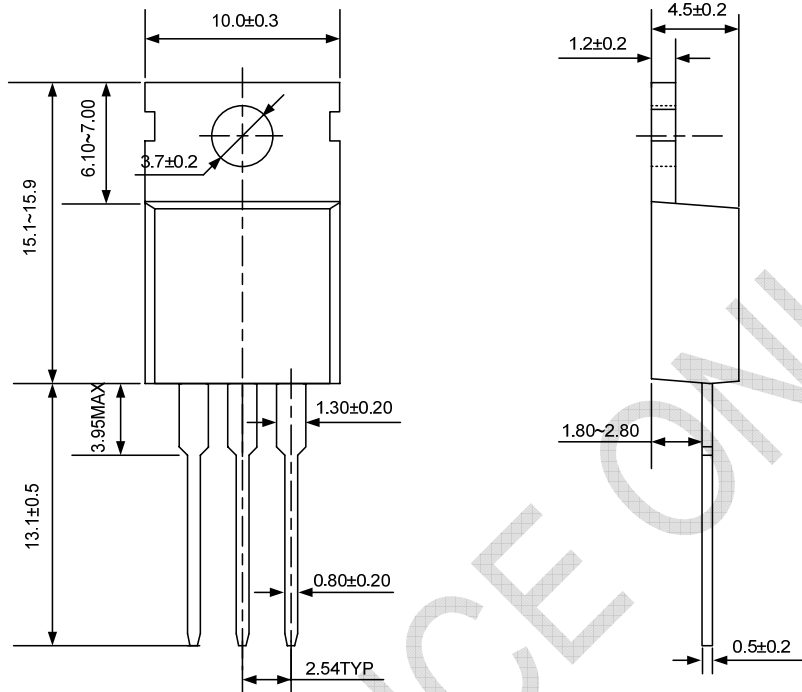

Resistive Switching Test Circuit & Waveform
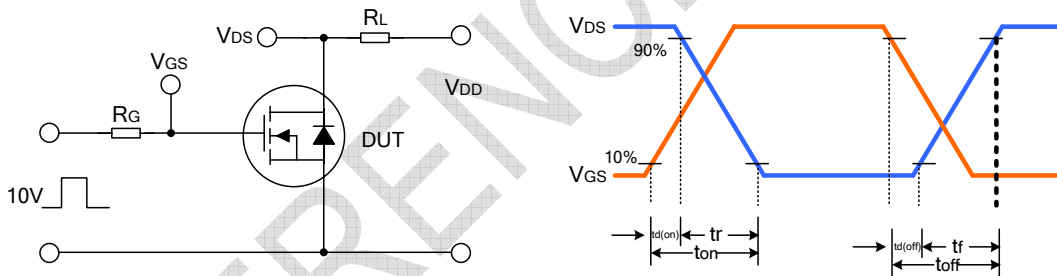
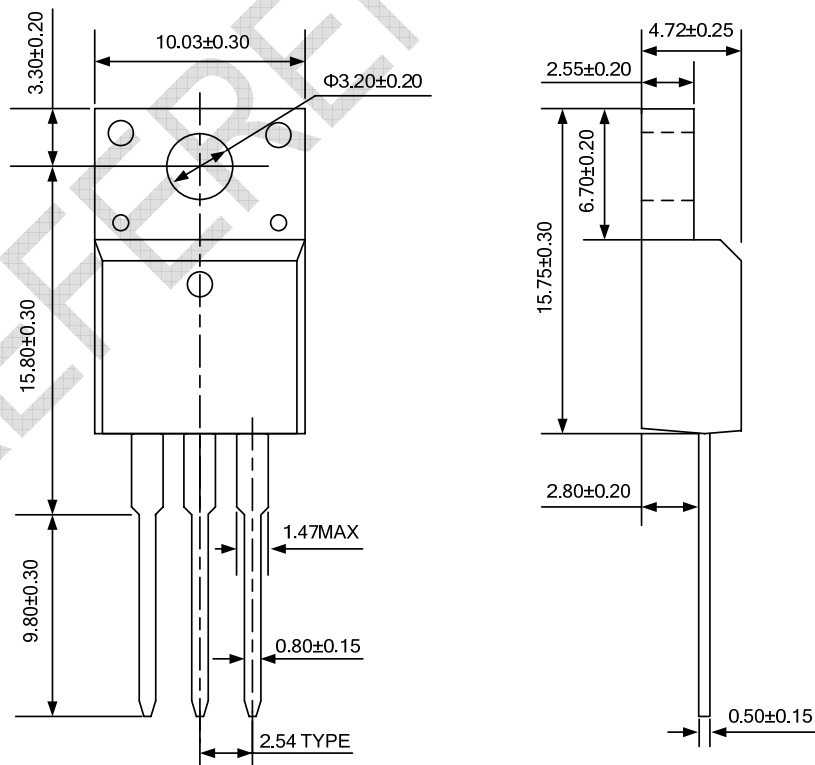Unclamped Inductive Switching Test Circuit & Waveform

$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{B_{VDSS}}{B_{VDSS} - V_{DD}}$$

PACKAGE OUTLINE

TO-220-3L UNIT: mm

TO-220F-3L UNIT: mm

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