# HIGH POWER FACTOR FLYBACK PWM CONTROLLER

## DESCRIPTION

SD7530 is a high power factor flyback PWM controller special for LED lighting applications.

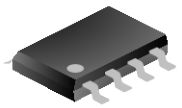
SD7530 features a high performance analog multiplier for power factor correction (PFC), zero current detector (ZCD) to ensure TM operation. It integrates a current sensing comparator with built-in leading-edge blanking, and a totem-pole output stage capable of -600mA /800mA current suited for big MOSFET.

SD7530 has a built-in soft-start circuit to avoid the over voltage output under light load start, reduce MOSFET's voltage stress, and improve circuit's reliability.

SD7530 has a built-in output short-circuit protection circuit, in this way the current of the system is considerably reduced to avoid the damage to IC.

SD7530 includes $V_{CC}$ under voltage lockout, $V_{CC}$ over voltage protection, over temperature protection, and AC input under-voltage and over-voltage protection, etc.

SD7530A has the same function and parameters with SD7530, except AC input undervoltage/overvoltage protection. (Unless otherwise stated, this document is only for SD7530)



SOP-8-225-1.27

## APPLICATIONS

* LED Daylight lamp

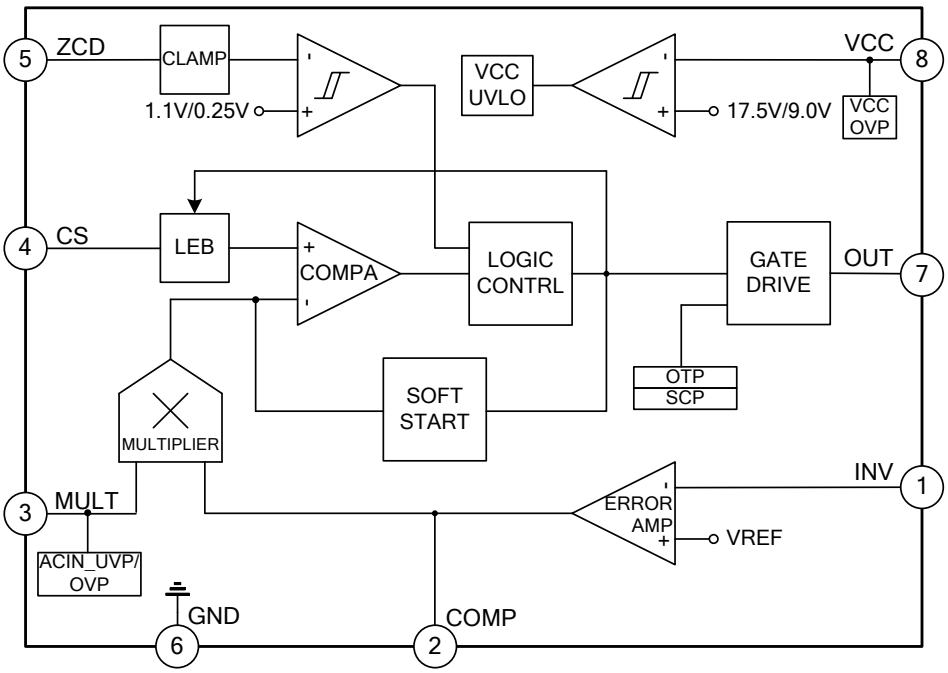
## FEATURES

* Transition Mode (TM) operation
* High-performance analog multiplier
* Built-in restart timer
* Integrate digital LEB
* Low start-up current (5μA)
* Audio noise free
* Built-in soft start circuit
* Very low power dissipation of output short-circuit protection (SCP)
* $V_{CC}$ under vltage lockout with hysteresis (UVLO)
* $V_{CC}$ over-voltage protection (VCCOVP)
* Over temperature protection (OTP)
* AC input under-voltage and over-voltage protection (ACIN_UVP/OVP)

## ORDERING INFORMATION

| Part No. | Package | Marking | Material | Packing |
|---|---|---|---|---|
| SD7530S | SOP-8-225-1.27 | SD7530S | Pb free | Tube |
| SD7530STR | SOP-8-225-1.27 | SD7530S | Pb free | Tape&Reel |
| SD7530AS | SOP-8-225-1.27 | SD7530AS | Pb free | Tube |
| SD7530ASTR | SOP-8-225-1.27 | SD7530AS | Pb free | Tape&Reel |

## BLOCK DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage ($I_{CC}$<20mA) | $V_{CC}$ | 40 | V |
| Peak drive output current | $I_{OH}/I_{OL}$ | -600/800 | mA |
| Voltage on analog input and output pins | - | -0.3 ~ 8 | V |
| Maximum current of zero current detector | - | ±10 | mA |
| Power dissipation (ambient temperature: 50°C) | $P_{diss}$ | 0.65 | W |
| Operating temperature range | $T_{amb}$ | -40~+120 | °C |
| Storage temperature range | $T_{stg}$ | -55~+150 | °C |
| Junction temperature | $T_j$ | +150 | °C |
| Thermal resistance from chip surface to the ambient | $R_{th(j-a)}$ | 150 | °C/W<br>°C/W |

**ELECTRICAL CHARACTERISTICS**(Unless otherwise stated, $V_{CC}$=22V；$C_O$=1nF；-25°C<$T_{amb}$<125°C)

| Characteristics | Symbol | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Power supply** | | | | | | |
| Operating voltage range | $V_{CC}$ | After start-up | 10.5 | -- | 32 | V |
| Turn-on threshold | $V_{CCon}$ | * | 16.5 | 17.5 | 18.5 | V |
| Turn-off threshold | $V_{CCoff}$ | * | 8.0 | 9.0 | 10.0 | V |
| Hysteresis voltage | $V_{CChys}$ | | -- | 8.5 | -- | V |
| Clamp voltage | $V_z$ | $I_{CC}$=20mA | -- | 40 | -- | V |
| VCC OVP | $VCC_{ovp}$ | | 32 | 34 | 36 | V |
| **Supply current** | | | | | | |
| Start current | $I_{ST}$ | Before start-up, $V_{CC}$=15V | -- | 5 | 10 | μA |
| Quiescent current | $I_Q$ | No switch | -- | 4 | 6 | mA |
| Operating current | $I_{CC}$ | f=70kHz | -- | 5 | 7 | mA |
| **Multiplier** | | | | | | |
| Input bias current | $I_{MULT}$ | $V_{MULT}$ = 0 ~ 4V | -- | -- | -1 | μA |
| Input voltage range | $V_{MULT}$ | Linear operation range | 0~3 | -- | -- | V |
| Gain ** | K | $V_{MULT}$=1V, $V_{COMP}$=4V | 0.32 | 0.38 | 0.44 | 1/V |
| Maximum output slope | $\frac{\Delta V_{CS}}{\Delta V_{MULT}}$ | $V_{MULT}$=0 ~ 1V<br>$V_{COMP}$=upper clamp voltage | 1.0 | 1.1 | -- | V/V |
| **Error amplifier** | | | | | | |
| Voltage feedback input threshold | $V_{REF}$ | $T_{amb}$=25°C | 2.45 | 2.5 | 2.55 | V |
| | | 10.5V< $V_{CC}$ <32V * | 2.44 | -- | 2.56 | |
| Linear regulation | - | $V_{CC}$ =10.5V~ 32V | -- | 2 | 5 | mV |
| Input bias current | $I_{INV}$ | $V_{INV}$ = 0 ~ 3V | -- | -- | -1 | μA |
| Voltage gain | $G_V$ | Open loop | 60 | 80 | -- | dB |
| Gain bandwidth product | $G_B$ | | -- | 1 | -- | MHz |
| Source current | $I_{COMP}$ | $V_{COMP}$=4V, $V_{INV}$=2.4V | -2 | -3.5 | -5 | mA |
| Sink current | $I_{COMP}$ | $V_{COMP}$=4V, $V_{INV}$=2.6V | 4 | 5.5 | 7 | mA |
| Upper clamp voltage | $V_{COMP}$ | $I_{source}$=0.5mA | 5.0 | 6.0 | 6.5 | V |
| Lower clamp voltage | $V_{COMP}$ | $I_{sink}$=0.5mA * | 2.0 | 2.25 | 2.4 | V |
| **Current sense comparator** | | | | | | |
| Input bias current | $I_{CS}$ | $V_{CS}$=0V | -- | -- | -1 | μA |
| Delay to output | $t_{d(H-L)}$ | | -- | 200 | 400 | ns |
| Current sense clamp | $V_{CS}$ | $V_{COMP}$=Upper clamp<br>$V_{MULT}$=1.5V | 1.0 | 1.08 | 1.16 | V |
| Current sense offset | $V_{offset}$ | $V_{MULT}$=0V | -- | 25 | -- | mV |
| | | $V_{MULT}$=2.5V | -- | 5 | -- | |
| **Zero current detector** | | | | | | |
| Input bias current | $I_{ZCD}$ | $V_{ZCD}$=1 ~ 4.5V | -- | 2 | -- | μA |
| Detect threshold | $V_{th(det)}$ | $V_{ZCD}$ rise *** | -- | 1.1 | -- | V |
| | | $V_{ZCD}$ fall *** | -- | 0.25 | -- | V |
| Detect hysteresis | HY(det) | *** | -- | 0.85 | -- | V |

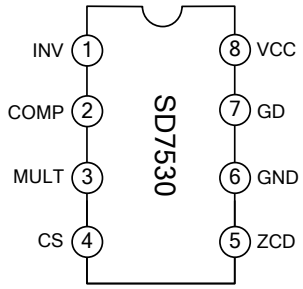
| Characteristics | Symbol | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Upper clamp voltage | $V_{ZCD}$ | $I_{ZCD}$=2.5mA | 6.3 | 6.8 | 7.3 | V |
| Lower clamp voltage | $V_{ZCD}$ | $I_{ZCD}$=-2.5mA | -0.3 | 0 | 0.3 | V |
| Source current capability | $I_{src}$ | | -2.5 | -- | -- | mA |
| Sink current capability | $I_{snk}$ | | 2.5 | -- | -- | mA |
| **Restart timer** | | | | | | |
| Restart timer period | $t_{d(rst)}$ | | 31 | 38 | 45 | μs |
| **Over Temperature Protection** | | | | | | |
| OTP | $T_{OTP}$ | | -- | 135 | -- | °C |
| Temperature hysteresis | $T_{HYS}$ | | -- | 15 | -- | °C |
| **Gate driver** | | | | | | |
| Output low voltage | $V_{OL}$ | $I_{sink}$=100mA | -- | 0.6 | 1.2 | V |
| Output high voltage | $V_{OH}$ | $I_{source}$=5mA | -- | 15 | -- | V |
| Peak drive source current | $I_{srcpk}$ | | -0.6 | -- | -- | A |
| Peak drive sink current | $I_{snkpk}$ | | 0.8 | -- | -- | A |
| Voltage rise time | $t_r$ | | -- | 70 | 110 | ns |
| Voltage fall time | $t_f$ | | -- | 40 | 70 | ns |
| Output clamp voltage | $V_{clamp}$ | $I_{source}$=5mA ; $V_{CC}$=32V | 12 | 15 | 18 | V |
| **AC input under-voltage and over-voltage protection** | | | | | | |
| MULT input under voltage protection threshold | $V_{MULTUVP1}$ | Driving output is off | -- | 0.95 | -- | V |
| MULT input under voltage get-out threshold | $V_{MULTUVP2}$ | Driving output is on | -- | 1.05 | -- | V |
| MULT input over voltage protection threshold | $V_{MULTOVP}$ | | -- | 4.50 | -- | V |
| MULT input under voltage lockout on delay | $t_{UVP1}$ | protection occurs - output shutdown | -- | 120 | -- | ms |
| MULT input under voltage lockout off delay | $t_{UVP2}$ | protection exits - output unlock | -- | 100 | -- | us |
| MULT input over voltage lockout on delay | $t_{OVP}$ | protection occurs - output shutdown | -- | 100 | -- | us |

* All the parameters are in tracking

** The multiplier output is given by: $V_{CS} = K \times V_{MULT} \times (V_{COMP} - 2.5)$

*** Parameters guaranteed by design.

## PIN CONFIGURATIONS




## PIN DESCRIPTIONS

| Pin No. | Pin Name | I/O | Description |
|---|---|---|---|
| 1 | INV | I | Inverting input of the error amplifier. The pin doubles as an ON/OFF control input. |
| 2 | COMP | I/O | Output of the error amplifier. A compensation network is placed between this pin and INV. |
| 3 | MULT | I | Main input to the multiplier. |
| 4 | CS | I | Input to the PWM comparator. The current flowing in the MOSFET is sensed through a resistor, the resulting voltage is applied to this pin. |
| 5 | ZCD | I | Input to the zero current detector. |
| 6 | GND | I/O | Ground. |
| 7 | GD | O | Gate driver output. |
| 8 | VCC | I/O | Supply voltage. |

## FUNCTION DESCRIPTION

SD7530 is a high power factor flyback PWM controller special for LED lighting applications. It operates in transition mode, it reduces the switch turn-on loss, improves the conversion efficiency and provides very good power factor correction.

### $V_{CC}$ UVLO and $V_{CC}$ OVP

Peripheral/internal circuit at pin Vcc of SD7530 is shown in figure 1. At the beginning of the power on, capacitor C1 is charged by $V_{IN}$ through start resistor R1, and $V_{CC}$ increases slowly. As $V_{CC}$ is up to 17.5V, IC starts to work and output driving pulse. Output voltage should be established in a period during which $V_{CC}$ discharges and diode D2 is reverse biased, and IC is fully powered by start capacitor C1. When output voltage increases to a certain value, diode D2 is forward conduction by auxiliary winding L3's voltage, and then $V_{CC}$ increases rapidly to the desired value. Fig. 2 shows the voltage waveform of $V_{CC}$ during start.
IC enters under voltage status as $V_{CC}$ is lower than 9.0V after start.
Moreover, the startup current of SD7530 is very low (less than 5uA), so large startup resistance R1 is recommended for low power dissipation.
If Vcc exceeds the internal reference 34V, IC enters over voltage protection (OVP), and turns off the PWM until next restart.

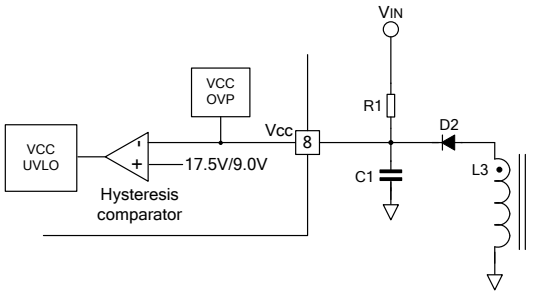



Fig.1 Internal /peripheral circuit at pin $V_{CC}$

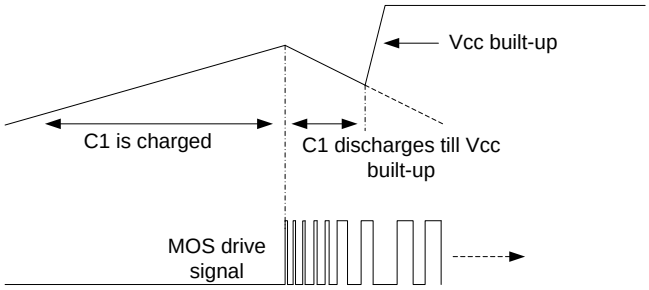



Fig. 2 the voltage waveform of $V_{CC}$ during start

## Error amplifier

Error amplifier of SD7530 and peripheral circuit are shown in fig.3. Error amplifier compares the voltage of pin INV which is fed back from output by optp-coupler with reference voltage (2.5V), amplifies the difference and outputs Vcomp. Generally, the bandwidth of PFC loop is less than 20Hz for better power factor correction, so compensation capacitor or resistor is connected between output (COMP) and inverting input (INV) of error amplifier in applications.

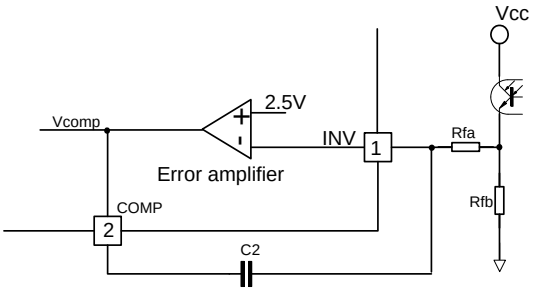



Fig.3 Error amplifier and peripheral circuit

## Multiplier and ACIN_UVP/OVP

Multiplier of SD7530 and peripheral/internal circuit are shown in figure 4. Input voltage $V_{IN}$ (output of rectifier bridge) is connected to input of multiplier through pin MULT after voltage dividing by R1a, R1b, and the other input of multiplier is output of error amplifier. Input voltage Vmult at pin MULT is half-sine voltage signal, but output voltage of multiplier Vmo is the half-sine voltage with same phase and different amplitude of input voltage Vmult, and controls the peak inductor current to change simultaneity, so that half-sine input average current is available.

Input and output of multiplier is expressed as:

$$Vmo = K \times Vmult \times (Vcomp - 2.5)$$

Where, K is the gain. (typical value for SD7530 is 0.38)

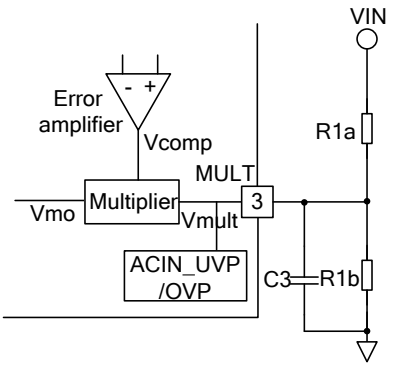



Fig.4 Multiplier and peripheral circuit

SD7530 has the undervoltage/overvoltage protection for AC input line voltage to enhance the security of IC and application system. AC line voltage $V_{IN}$ is detected by the input pin MULT of the multiplier. When Vmult is lower than 0.95V, IC enters undervoltage protection and turns off PWM after 120ms, then the system stops working; when Vmult is higher than 1.05V, IC exits undervoltage protection and turns on PWM after 100us, then the system restarts automatically and resumes normal working. When Vmult is higher than 4.5V, IC enters over voltage protection and turns off PWM after 100us, and the system stops working; when Vmult is lower than 4.5V, IC exits overvoltage protection and turns on PWM directly, then the system restarts automatically and resumes normal working.

The formula is shown below:

$$Vmult = \sqrt{2} \times Vin \times \frac{R1b}{R1a + R1b}$$

### Inductor current detection (turn off MOSFET)

Current sense comparator of SD7530 and peripheral circuit are shown in figure 5. It is used for detecting inductor peak current to turn off MOSFET and make the system to stop working. Sense resistor Rs is connected between source of MOSFET and ground, and the voltage of sense resistor can be behaved on inductor current, which acts as the non-inverting input of current sense comparator through pin CS, compared with output of multiplier, which acts as the inverting input. If peak voltage of sense resistor increases to the limited value of multiplier output, current sense comparator's output overturns to turn off MOSFET.

LEB is added at pin CS to chops off the sense voltage spike at MOSFET on state due to snubber diode reverse recovery.

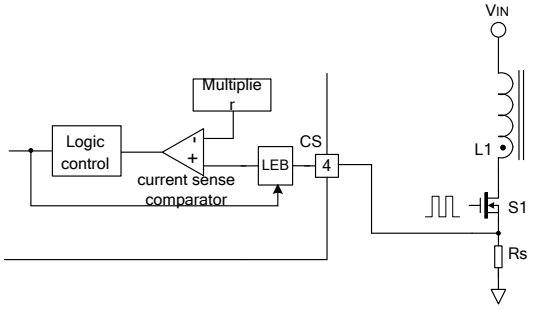



Fig 5. Current sense comparator and peripheral circuit

### Zero current detection (turn on MOSFET)

Zero current comparator of SD7530 and peripheral circuit are shown in Fig.6. Zero current detector is used for detecting zero-crossing of inductor current and turning on MOSFET. Dotted terminal of auxiliary winding L3 is connected to pin ZCD via a resistor Rzcd. When inductor current decreases to zero, voltage at dotted terminal is lower than 0.25V, gate drive signal of MOSFET turns to high and MOSFET is turned on, and 0.85V hysteresis is set to avoid error actions.

Clamp circuit at pin ZCD clamps the voltage in 0V~6.0V.

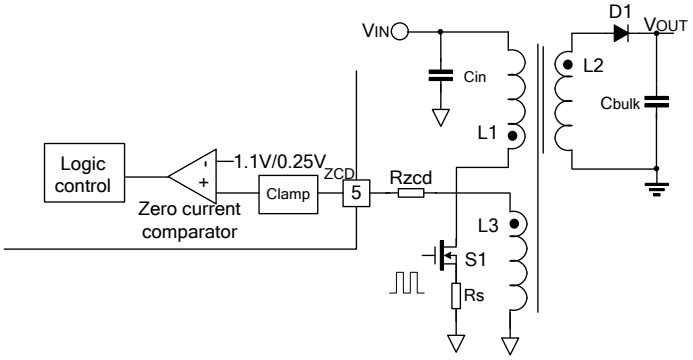



Fig. 6 Zero current comparator and peripheral circuit

Fig. 7 shows the detailed voltage waveforms for zero current detection. After MOSFET is turned off and before the inductor current decreases to zero, the voltage at pin ZCD keeps high and is given as:

$$V_{ZCD} = \frac{(Vo - Vin)}{n}$$

Where, n is the turns ratio of the primary windings L1 and auxiliary windings L3.

During MOSFET off but inductor current is not zero, the inductor current is supplied to the load through secondary winding L2 and diode D1, and decreases linearly to zero, at the mean while the diode D1 is reverse blocked and MOSFET S1 junction capacitor is resonant with the primary windings L1 and input capacitor Cin. Then the drain voltage of MOSFET is going down, voltage at pin ZCD also decreases. When the drain voltage decreases to $V_{IN}$, the voltage at dotted terminal of auxiliary winding L3 is zero. Due to MOSFET is still off, the drain voltage continuously decreases until the voltage at pin ZCD is lower than 0.25V, then MOSFET is on. When the drain voltage decreases to zero, the resonance stops and the inductor current increases linearly.

As shown in Fig. 7 below, this characteristic allows turning on MOS with low voltage for decreasing the switch turn-on loss

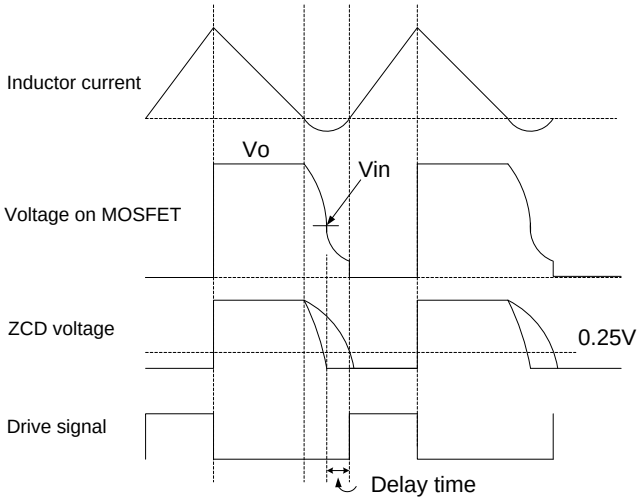



Fig. 7. The detailed voltage waveforms for zero current detection

### Output short-circuit protection

SD7530 integrates output short-circuit protect(SCP) circuit. If output load's short-circuit state is detected by IC, PWM will be turned off automatically, and $V_{CC}$ will gradually decrease until IC restarts automatically.

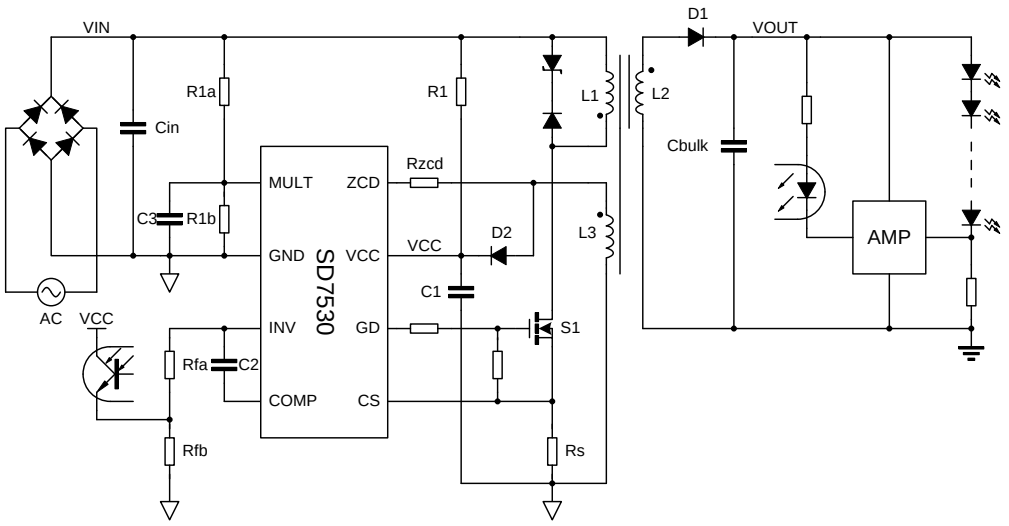
### Soft start

SD7530 integrates soft-start circuit, which is used to reduce the voltage stresses and current surges of IC during start up. This circuit first clamps the output voltage of multiplier at a low level, then improves the output voltage gradually during start up. So that PWM can increase gradually from zero to the steady state.

### Over temperature protection

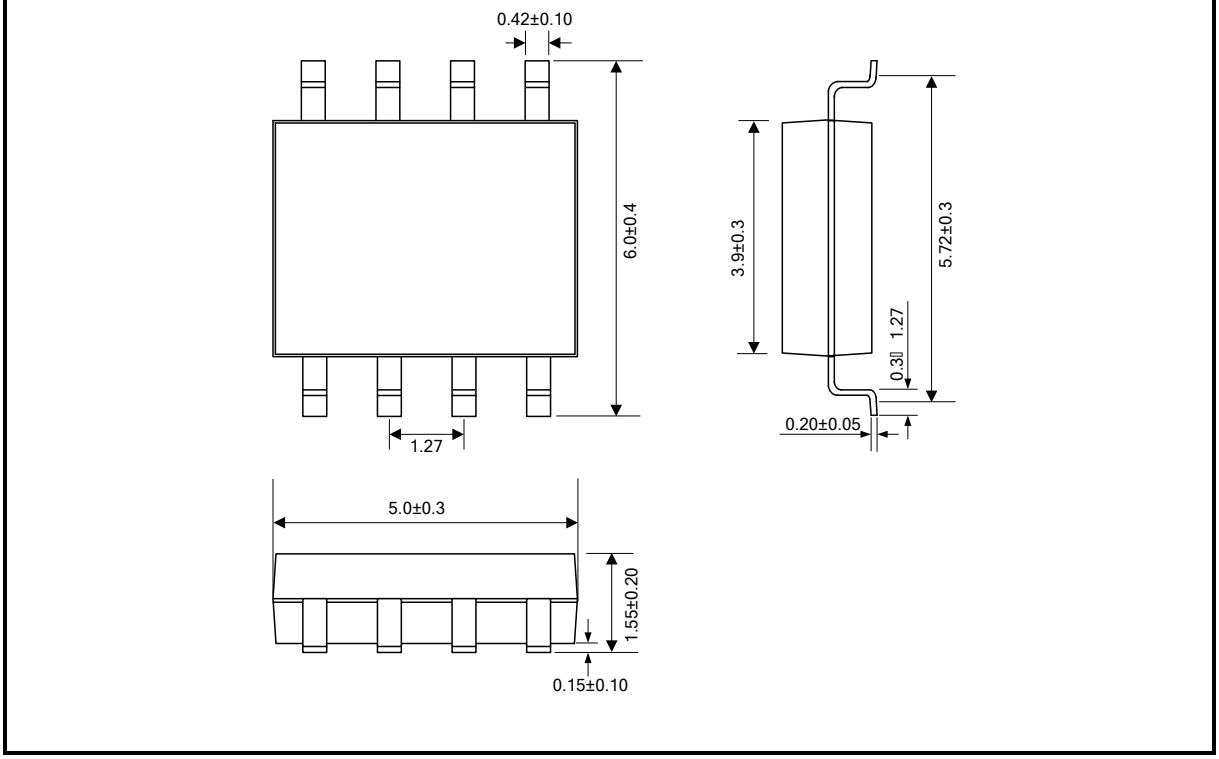
SD7530 integrates over temperature protect(OTP) circuit. IC is shutdown when the temperature is higher than 135°C and recovers when temperature decreases to 120°C.

## TYPICAL APPLICATION CIRCUIT



## PACKAGE OUTLINE

SOP-8-225-1.27 UNIT: mm





### MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

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## ATTACHMENT

### Revision History

| Date | REV | Description | Page |
|---|---|---|---|
| 2012.10.25 | 1.0 | Initial release | |